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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/634,153
Filing Date: August 04, 2003
Appellant(s): PARKINSON ET AL.

Ward D. Parkinson
For Appellant

EXAMINER'S ANSWER

This is in response to the amended brief filed Oct 16, 2006 appealing from the Office action mailed 2/16/2006.

(1) Real Party in Interest

The real party in interest is the assignee Ovonyx, inc.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

The following grounds of rejection are presented for review on appeal:

B. Are claims 1-25 unpatentable over Ovshinsky?

C. Are claims 1-25 unpatentable over Klersy?

D. Are claims 1-25 unpatentable over Czubatyj 6046?

E. Are claims 1-17 & 19-25 unpatentable over Van Brocklin?

F. Are claims 1-19 & 21-25 unpatentable over Czubatyj :340?

The following grounds of rejection are not presented for review on appeal because they have been **withdrawn** by the examiner.

A. Are claims 2, 11, 12, 14-16, and 22-25 indefinite for failing to particularly point out and distinctly claim the subject matter of the invention?

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied On

The following U.S patents are relied on by the examiner :

- **Ovshinsky (RE 37,259), filed 11/08/1999, issued 07/31/2001**
- **Klersy et al (US 5,933,365), filed 06/19/1997, issued 08/03/1999**
- **Czubatyj (US 5,825,046), filed 10/28/1996, issued 10/20/1998**
- **Van Brocklin et al (US 6,879,525), filed 10/31/2001, issued 04/12/2005**
- **Czubatyj (US 4,782,340), filed 08/22/1986, issued 11/01/1988**

(9) Grounds of Rejection

B. Claims 1-25 are rejected under 35 U.S.C 103(a) as being unpatentable over Ovshinsky (RE 37,259).

Ovshinsky (RE37259) patent, col. 1 (lines 26-27) from this patent specifically stated that "**Ohvonic EEPROM** is capable of storing **both analog and digital forms of information**" for storage (emphasis added). Thus, the pure knowledge of using phase-change material to store analog signal/information, besides digital values, has been previously known and widely acknowledged; and therefore, one skilled in the art can use this patent disclosure to make/produce a memory **to store only data/information in the analog form (without any digital states or A/D conversions)** if desired. It is noted that even though Ovshinsky patent teaches his memory as **capable of storing both analog and digital information** and not limited to only analog data type as claim 1, one having ordinary skill in the art can still utilize his structure to store only one type of data/information, i.e.. either chosen digital or analog type, and thus as a result, the whole memory structure could be called by a skilled artisan as either a "**digital memory**" or a pure "**analog memory**" if one desired without further modification and/or complex design changes. Furthermore, the term "analog memory" or "digital memory" can be interpreted or construed as a memory structure capable of storing either analog or digital, but not both at same time.

Regarding claims 2-7 & 12-16, & 22-25, this patent clearly teaches away the applicant's claims **2 & 7** because both these claims also specifically reciting that **information/data can be stored in either digital or analog form (see claim 2)** and also **in at least three different resistance values (see claim 7)** which is also consistent with the disclosure of this patent's suggestion in terms of a wide range of number of states detected by changed resistances from each memory cell (i.e., gray scale or pseudo-analog);

Regarding claims 8-10, col. 20 described in detail how the current magnitude for programming the cell could vary as the cell resistance varies thus obviously suggesting its resistance value as proportional to either a current or voltage characteristic to be stored into the cell.

Regarding claim 11, 17, & 19, the "signal generating means" and "addressing matrix" mentioned on col. 19 (lines 15-21) would obviously constitute the claimed circuit including sense amplifier and read/write circuitry for reading and writing analog data.

Regarding claim 18, "pore" definition and use is disclosed on col. 17 (lines 1-12).

Regarding claim 20, chalcogenide material is mentioned on col. 7 (line 67).

Regarding claim 21, the use of a "processor" or a "wireless interface" in combination with any memory type, including a phase change material, would be obvious to one skilled in this art.

C. Claims 1-25 are rejected under 35 U.S.C 103(a) as being unpatentable over Klersy et al (5,933,365).

Klersy et al patent, col. 1 (lines 20-22) from this patent specifically stated that "**Ohvonic EEPROM** is capable of storing **both analog and digital forms of information**" for storage (emphasis added). Thus, the pure knowledge of using phase-change material to store analog signal/information, besides digital values, has been previously known and widely acknowledged; and therefore, one skilled in the art can use this patent disclosure to make/produce a memory **to store only data/information in the analog form (without any digital states or A/D conversions)** if desired. It is noted that even though Klersy patent teaches his memory as **capable of storing both analog and digital information** and not limited to only analog data type as claim 1, one having ordinary skill in the art can still utilize his structure to store only one type of data/information, i.e.. either chosen digital or analog type, and thus as a result, the whole memory structure could be called by a skilled artisan as either a "**digital memory**" or a pure "**analog memory**" if one desired without further modification and/or complex design changes. Furthermore, the term "analog memory" or "digital memory" can be interpreted or construed as a memory structure capable of storing either analog or digital, but not both at same time.

Regarding claims 2-7 & 12-16, & 22-25, this patent clearly teaches away the applicant's claims **2 & 7** because both these claims also specifically reciting that **information/data can be stored in either digital or analog form (see claim 2)** and also **in at least three different resistance values (see claim 7)** which is also consistent with the disclosure of this patent's suggestion in terms of a wide range of number of states detected by changed resistances from each memory cell (i.e., gray

scale or pseudo-analog). Particularly, col. 18 (lines 1-13) discussed the use of a "dynamic" range of sub-ranges of resistances that can allow the creation of any multi-level analog memory.

Regarding claims 8-10, col. 3 described in detail how the switching current required for programming the cell can vary as the cell resistance varies thus obviously suggesting its resistance value as proportional to either a current or voltage characteristic to be stored into the cell.

Regarding claim 11, 17, & 19, the addressing lines and circuitry mentioned on col. 17 (lines 1-14) would obviously constitute the claimed circuit including sense amplifier and read/write circuitry for reading and writing analog data, if any.

Regarding claim 18, "pore" definition and use is disclosed on col. 15 (lines 24-39).

Regarding claim 20, chalcogenide material is mentioned on col. 5 (line 45).

Regarding claim 21, the use of a "processor" or a "wireless interface" in combination with any memory type, including a phase change material, would be obvious to oen skilled in this art.

D. Claims 1-25 are rejected under 35 U.S.C 103(a) as being unpatentable over Czubatyj et al (US 5,825,046).

Czubatyj patent, col. 1 (lines 26-27) from this patent specifically stated that "**Ohvonic EEPROM** is capable of storing **both analog and digital forms of information**" for storage (emphasis added). Thus, the pure knowledge of using phase-

change material to store analog signal/information, besides digital values, has been previously known and widely acknowledged; and therefore, one skilled in the art can use this patent disclosure to make/produce a memory **to store only data/information in the analog form (without any digital states or A/D conversions)** if desired. It is noted that even though Czubatyj patent teaches his memory as **capable of storing both analog and digital information** and not limited to only analog data type as claim 1, oen having ordinary skill in the art can still utilize his structure to store only one type of data/information, i.e.. either chosen digital or analog type, and thus as a result, the whole memory structure could be called by a skilled artisan as either a "**digital memory**" or a pure "**analog memory**" if one desired without further modification and/or complex design changes. Furthermore, the term "analog memory" or "digital memory" can be interpreted or construed as a memory structure capable of storing either analog or digital, but not both at same time.

Regarding claims 2-7 & 12-16, & 22-25, this patent clearly teaches away the applicant's claims **2 & 7** because both these claims also specifically reciting that **information/data can be stored in either digital or analog form (see claim 2)** and also **in at least three different resistance values (see claim 7)** which is also consistent with the disclosure of this patent's suggestion in terms of a wide range of number of states detected by changed resistances from each memory cell (i.e., gray scale or pseudo-analog);

Regarding claims 8-10, col. 14 described in detail how the current magnitude for programming the cell could vary as the cell resistance varies thus obviously suggesting

its resistance value as proportional to either a current or voltage characteristic to be stored into the cell.

Regarding claim 11, 17, & 19, the "signal generating means" and "addressing matrix" mentioned on col. 13 (lines 52-60) would obviously constitute the claimed circuit including sense amplifier and read/write circuitry, etc., for reading and writing analog data.

Regarding claim 18, "pore" definition and use is disclosed on col. 11 (line 55).

Regarding claim 20, chalcogenide material is mentioned on col. 5 (line 47) & col. 14.

Regarding claim 21, the use of a "processor" or a "wireless interface" in combination with any memory type, including a phase change material, would be obvious to oen skilled in this art.

E. Claims 1-17, 19-25 are rejected under 35 U.S.C 103(a) as being unpatentable over Van Brocklin et al (US 6,879,525).

Van Brocklin et al (see Fig. 3) teaches the use of a phase-change material with changeable resistance (element 52) to be programmed by the applied current/voltage device 70) in order to store the magnitude of information representing the data in analog form. Information read out can then be detected and/or written by measured using the read-out current using the DAC (digital-to-analog converter unit 80) through read-out resistor element (74). Thus, since read out current going through the programmable resistor (52) from each cell is already in the analog form (***even though this patent***

does not specifically spelled out that analog is the only stored form allowed), it still would have been obvious to one skilled in this art that by changing the magnitude of such applied voltage or applied current (with continuous varying values/waveforms) going through the op-amp (66) and into the cell (56), any amount of analog data can be stored in terms of its continuous varying analog voltage levels and/or amplitudes instead of just pure digital levels/states as compared with other conventional non-volatile, threshold memory devices. For example, col. 2(lines 55-67) stated that the **electrical parameters** such as, i.e., voltage or current going through each stored cell is continuous because it is handled by a current **continuously feedback device**. Thus, each cell is not stored in terms of states but can be used to store in multiple states or continuous varying (current) levels if desired. Furthermore, when/if any digital values/states are to be used, col. 5 (lines 32-37) sated that "any amount of states could theoretically be implemented.." thus also obviously suggest that an unlimited amount or continuous varying range of voltage levels can be stored, which also means that the whole range of analog voltage levels that a resistor can store to represent any data in any analog form/level as well, etc. Finally, Fig. 4 also shows that the stored current value, if any, of memory cell (**see predetermined value C, Figs. 3 & 4**) read out form each cell is also "**continuously varying**" with "continuously" increasing values over the programming period because the shape of its current waveform is analog changing with stair-case increasing values, and thus has no stored "**discrete**" or "**gray scale**" states, etc.

Regarding other claimed features concerning the use of sense amplifier, read/write devices or current control devices using current sensing techniques are obviously seen in Figs. **2, 3, & 6** of this patent.

Regarding claims 8-10, Fig. 1 shows the relationship between device current and memory cell state change thus it shows how the current magnitude for programming the cell can vary as the cell resistance varies, and thus obviously suggesting its resistance value as proportional to either a current or voltage characteristic to be stored into the cell.

Regarding claim 11, 17, & 19, Fig. 2 clearly shows the claimed memory circuit including sense amplifier, addressing, and read/write circuitry, etc., for reading and writing analog data.

Regarding claim 20, chalcogenide material is mentioned on col. 3 (line 67).

Regarding claim 21, the use of a "processor" or a "wireless interface" in combination with any memory type, including a phase change material, would be obvious to oen skilled in this art.

F. Claims 1-19 & 21-25 are rejected under 35 U.S.C 103(a) as being unpatentable over Czubatyj (4,782,340).

Czubatyj (see Fig. 1) teaches the use of a phase-change material (i.e., col.2, lines 65-68) inside a memory cell to store data by programming its **continuously varying resistance values** to represent multitude of data levels. It is noted even though this patent does not stated specifically that its memory design can be used to store only

in "analog" form. Yet, **col. 2 (lines 25-35)** specifically stated that information **can be stored in by applied signals or waveforms, or in any other analog forms, or in any other electrically detectable form**, etc., thus obviously indicate to one skilled in this art the other possibility of using applied currents or applied voltages for storing/transforming these direct values into the cell resistance values (& in only analog form) as another alternative, if desired. Detected or read-out currents, if any, thus can be interpreted as analog or converted into digital states if desired. However, the stored data must be in analog forms (as it is in the forms of continuously current or analog values only).

Regarding other claimed features concerning the use of sense amplifier, read/write devices or current control devices using current sensing techniques are obviously seen in Figs. **4, 6, 8, 10, & 32** of this patent.

Regarding claims 8-10, col. 2 described in detail how the current magnitude for programming the cell could vary as the cell resistance varies thus obviously suggesting its resistance value as proportional to either a current or voltage characteristic to be stored into the cell.

Regarding claim 11, 17, & 19, Fig. 32 shows the claimed circuit including sense amplifier, decoder, addressing, and read/write circuitry, etc., for reading and writing analog data.

Regarding claim 18, "pore" definition and use is disclosed on col. 23-24.

Regarding claim 21, the use of a "processor" or a "wireless interface" in combination with any memory type, including a phase change material, would be obvious to oen skilled in this art.

10) Response to Argument

With regard to all the above cited patents, the appellant maintains that their disclosed memory devices can not store analog signals but only digital states and/or gray scale levels of information thus can not teach the claims. However, as clearly shown above and reasoned in detail in earlier office actions, the examiner disagrees because the fact that they can store both, i.e., digital data besides analog data, or they can choose to store only one type of information (digital or analog) if desired, and because the fact that at least the three patents of Ovshinsky, Klersy, and Czubatyj clearly stated that their memories can store **both analog and digital information** thus obviously imply the desired choices of data storage structure and/or appropriate types of data (analog or digital) can be stored separately or altogether in that structure as well. However, the language of independent claim 1 & 11 broadly citing the word "analog memory", which could be interpreted by the examiner as a memory with an intended purpose of capable of storing analog information only (besides digital) as one type of information choice, which is also implied by the above patents' statements as one choice of data type storage.

Lastly, the patent of Van Brocklin et al (Fig. 3) and Czubatyj (Fig. 1) teaches the use of resistor inside each cell and continuous changing currents going through each

resistor, and one having ordinary skill in the electrical and electronics technology would readily understood that as the current going through each cell is changing, its resistance values is changing as well, thus causing the cell structure having many possible ***continuous analog signal values***, for example, i.e., based on the electrical equation of **R = V/I**, ***where V is the varying analog values of cell voltage, I is the varying analog values of cell current, and R is the fixed analog resistance values for example.*** Even though the patents might convert these analog current-voltage values into digital storage state as their end results, the appellant's arguments are still not persuasive and convincing because the patent's structure is already capable of storing analog signal values by just using these resistors and phase change material without implying the end results, and thus its structure would have been obvious to one having ordinary skill in the art as the so-called type of "**analog memory**" structure. Furthermore, one having ordinary skill in the art would readily understand that at least Van Brocklin patent (**Fig. 1**) shows this linear relationship between cell' current and cell's voltage as a continuous signal line and thus the cell storage structure is not only limited to just capable of storing "**distinct, digital storage states**" (as end results) as asserted by the appellant because it can carry analog current as well.

The above rejections still stand and are maintained by the examiner.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Viet Q. Nguyen

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